IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A grid array signal conducting arrangement comprising at least one differential grid array conductor pair and at least one non-differential grid array conductor pair, the at least one differential grid array conductor pair having portions thereof which are more closely spaced in comparison to a spacing of corresponding components in the at least one non-differential grid array conductor pair.

2. (Original) A grid array signal conducting arrangement as claimed in claim 1, where the grid array signal conducting arrangement is provided in a grid array connector provided on at least one of a receiving substrate and a semiconductor package.

3. (Original) A grid array signal conducting arrangement as claimed in claim 1, where the grid array signal conducting arrangement conducts at least one differential pair signal.

4. (Original) A grid array signal conducting arrangement as claimed in claim 3, where the grid array signal conducting arrangement provides at least one of greater coupling and greater common noise between the differential grid array conductor pair than the non-differential grid array conductor pair.

5. (Currently Amended) A grid array signal conducting arrangement comprising:

at least one differential grid array conductor pair and at least one non-differential grid array conductor pair; and

means for providing noise rejection capability in the grid array signal conducting arrangement while increasing coupling within the at least one differential grid array conductor pair and decreasing coupling within the at least one non-differential grid array conductor pair.

6. (Original) A grid array signal conducting arrangement as claimed in claim 5, where the grid array signal conducting arrangement is provided in a grid array connector provided on at least one of a receiving substrate and a semiconductor package.

7. (Original) A grid array signal conducting arrangement as claimed in claim 5, where the grid array signal conducting arrangement conducts at least one differential pair signal.

8. (Original) A grid array signal conducting arrangement as claimed in claim 7, where the grid array signal conducting arrangement provides at least one of greater coupling and greater common noise between the differential grid array conductor pair than the non-differential grid array conductor pair

A2

9. (Original) An electrical component comprising:

at least one of a receiving substrate and a semiconductor package; and

a grid array signal conducting arrangement comprising at least one differential grid array conductor pair and at least one non-differential grid array conductor pair, the at least one differential grid array conductor pair having portions thereof which are more closely spaced in comparison to a spacing of corresponding components in the at least one non-differential grid array conductor pair.

10. (Original) An electrical component as claimed in claim 9, where the grid array signal conducting arrangement conducts at least one differential pair signal.

11. (Original) An electrical component as claimed in claim 10, where the grid array signal conducting arrangement provides at least one of greater coupling and greater common noise between the differential grid array conductor pair than the non-differential grid array conductor pair.

12. (Original) A mounted electrical component arrangement comprising:

a plurality of electrical components; and

a grid array signal conducting arrangement comprising at least one differential grid array conductor pair and at least one non-differential grid array conductor pair, the at least one differential grid array conductor pair having portions thereof which are more closely spaced in comparison to a spacing of corresponding components in the at least one non-differential grid array conductor pair.

13. (Original) A mounted electrical component arrangement as claimed in claim 12, where the grid array signal conducting arrangement is provided in a grid array connector provided on at least one of a receiving substrate and a semiconductor package.

A2

14. (Original) A mounted electrical component arrangement as claimed in claim 12, where the grid array signal conducting arrangement conducts at least one differential pair signal.

15. (Currently Amended) A mounted electrical component arrangement as claimed in claim 14, where the grid array signal conducting arrangement provides at least one of greater coupling and greater common noise between the differential grid array conductor pair than the non-differential grid array conductor ~~pa~~ pair.

16. (Currently Amended) A method of increasing noise rejection capability of a grid array signal conducting arrangement comprising:

orientating electrical conductive parts in the grid array signal conducting arrangement that conduct differential signals so that a ~~as~~ coupling distance between at least one pair of differential signals is less than coupling distance between at least one pair of non-differential signals; and

conducting at least one pair of differential signals through the electrical conductive parts.

17. (Original) A method as claimed in claim 16, where the grid array signal conducting arrangement is provided in a grid array connector provided on at least one of a receiving substrate and a semiconductor package.

Please add the following claims:

18. (New) A grid array signal conducting arrangement as claimed in claim 5 wherein the means for providing noise rejection capability in the grid array signal conducting arrangement includes orientating electrical conductive parts in the grid array signal conducting arrangement such that a coupling distance between at least one pair of differential signals is less than a coupling distance between at least one pair of non-differential signals.

A3

19. (New) A grid array signal conducting arrangement comprising:

a differential grid array conductor pair and a non-differential grid array conductor pair, the non-differential grid array conductor pair having pin/socket connection areas spaced more closely in comparison to a spacing of pin/socket connection areas in the differential grid array conductor pair.

20. (New) A grid array signal conducting arrangement comprising:

a differential grid array conductor pair and a non-differential grid array conductor pair, the differential grid array conductor pair having socket plates spaced more closely in comparison to a spacing of socket plates in the non-differential grid array conductor pair.

21. (New) A flip chip pin grid array of a grid array signal conducting arrangement comprising a plurality of pins that are received into corresponding sockets of a substrate, wherein the pins are spaced as shown in Fig. 5.

22. (New) A flip chip pin grid array as in claim 21, wherein the pins are in pairs and each of the pairs are spaced from each other.

23. (New) A substrate of a grid array signal conducting arrangement comprising a first socket member, a second socket member, and a third socket member in between the first and second socket members, wherein the third socket member is oriented at 180° from the first and second socket members.

24. (New) A substrate as in claim 23 wherein the first and third socket members form a portion of a differential pair, and the third and second socket members form a portion of a non-differential pair, wherein a distance between a socket plate of the first socket member and a socket plate of the third socket member is smaller than a distance between a socket plate of the second socket member and the socket plate of the third socket member.

A3

25. (New) A grid array signal conducting arrangement comprising:

a differential grid array conductor pair having a first socket plate and a corresponding first pin/socket connection area, and having a second socket plate and a corresponding second pin/socket connection area; and

a non-differential grid array conductor pair,

wherein the first and second socket plates are both in between the first and second pin/socket connection areas.

26. (New) A grid array signal conducting arrangement as in claim 25 wherein the non-differential grid array conductor pair includes the second socket plate and the corresponding second pin/socket connection area, and also has a third socket plate and a corresponding third pin/socket connection area, wherein the second and third pin/socket connection areas are in between the second and third socket plates.